corresponding video data addresses within a predetermined address range;

a display memory controller, coupled to said bus interface, ***for receiving video data in a component YUV format in contiguous successive streams of luminance and chrominance difference data and corresponding video data addresses within a predetermined address range and for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory;*****.....**

wherein said display memory controller stores the first contiguous block of luminance data in at least one byte lane within the display memory and stores the at least a second contiguous block of chrominance difference data in at least another byte lane within the display memory. (emphasis added)

The claimed invention beneficially provides a display controller that can assist a host processor in decoding MPEG data. The display controller receives YUV data in non-pixel video format from a host CPU and performs the otherwise CPU intensive task of rasterization. Thus, the display controller beneficially takes the rasterization chore away from an MPEG decoder in the host processor by making

clever use of memory apertures to store the data directly into video pixel. Additionally, the memory aperture used to store data is "a hitherto unused display memory address aperture" and thus the display controller can maintain compatibility with the PCI bus standard and prior art display controller software and hardware." (see specification, page 20, lines 11-15).

The claimed invention is not disclosed or suggested by Hancock '514, Munson '277, Coelho '137, and Selwan '025, either alone or in combination. Hancock '514 discloses a data processing system 10 that includes a video memory access controller 28, a video memory 30, a video display controller 32, a DAC 34, and a monitor 36. (col. 3, lines 25-29). The video memory access controller 28 provides pixel data values and pixel state values to the video memory 30 (see Fig. 1 of Hancock '514). The video memory 30 comprises a pixel data region 38 and a pixel state mask 40 defining the state of each pixel, and the controller 32 continuously accesses the pixel data in video memory 30 one pixel at a time and decides the color for a pixel. (col. 3, lines 34-36 and col. 4, lines 7-9). The pixel state mask determines how the video controller

32 is to interpret the pixel data for that pixel and thus allows the concurrent display of graphics and image data. (col. 2, lines 49-53). Hancock '514 does not disclose or suggest, as recited in claim 1, a display memory controller with the following features and capabilities: ***(1) receiving video data in a component YUV format in contiguous successive streams of luminance and chrominance difference data and corresponding video data addresses within a predetermined address range; and (2) storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory; and (3) storing the first contiguous block of luminance data in at least one byte lane within the display memory and storing the at least a second contiguous block of chrominance difference data in at least another byte lane within the display memory.*** Therefore, the Applicant respectfully submits that claim 1 is patentably distinguishable over Hancock '514.

The Examiner also correctly states that Hancock '514 fails to expressly teach a bus interface means coupled to the

data bus. In an attempt to overcome the deficiency of Hancock '514, the Examiner relies on Munson '277 to show a PCI interface block 109 coupled to a PCI bus 115.

Munson '277 discloses an embodiment 100 that "serves as the interface between a National Television Standards Committee (NTSC)/Phase Alternation Line (PAL)/SECAM digital video decoder/scaler 117 and a Peripheral Component Interconnect (PCI) local bus 115 of a personal computer." (col. 5, lines 58-63). The PCI interface block (PIB) 109 "operates as a PCI bus master when the video DMA controller [106] is delivering captured video images to the PCI memory 111, the RPS 108 is accessing PCI memory 111 for register value lists or writing data, and the DCI block 103 is fetching data." (col. 26, lines 25-33) (emphasis added). Munson '277 does not disclose or suggest, as recited in claim 1, a display controller including: a ***bus interface***, coupled to the data bus, ***for receiving video data in a component YUV format*** and ***corresponding video data addresses within a predetermined address range***.

Furthermore, there is no suggestion or incentive to combine Hancock '514 and Munson '277 for the following

reasons. First, the graphics coprocessor 20 in Hancock '514 transfers blocks of pixel data (via bus 22) between the system memory 14 and the video memory 30 in response to "control commands" from main processor 12. (col. 3, lines 19-25). A video memory access controller 28, which is coupled to graphics coprocessor 20, automatically sets corresponding locations of pixel state mask 40 as pixel data is written into video memory 30, in accordance with the setting of a register 42. (col. 4, lines 43-46). Therefore, by connecting the PCI interface block 109 of Munson '277 to the bus 22 to replace the video memory access controller 28, the basic principle under which Hancock '514 was designed to operate would change since it is believed that the PCI interface block 109 would be unable to automatically set corresponding locations of pixel state mask 40. (See MPEP 2143.01). Therefore, the combination of Hancock '514 and Munson '277 is improper.

Furthermore, there is no incentive to combine Hancock '514 and Munson '277 based on the following teaching in Hancock '514. The graphics coprocessor 20 performs functions such as transferring blocks of pixels between system memory 14 and video memory 30. Thus, the graphics coprocessor 20

controls the data transfers between itself and the system memory 14 along bus 22. Similarly, the PCI interface block 109 of Munson '277 operates as a PCI bus master. (col. 26, lines 29-34). A "bus master" is a device or subsystem that controls data transfers between itself and a slave. (see IBM Dictionary of Computing, McGraw-Hill, Inc., page 77, 1994). Thus, there is no incentive to add the PCI interface block 109 of Munson '277 to the bus 22 of Hancock '514 since the graphics coprocessor 20 already controls data transfer from system memory 14 and along bus 22.

Furthermore, there is no incentive to combine Hancock '514 and Munson '277 since such combination would require a substantial reconstruction of the elements shown in Hancock '514 and/or would result in a non-operative embodiment for the following reasons. First, the graphics coprocessor 20 of Hancock '514 is configured to receive control commands from main processor 12 in order to transfer data from system memory 14 to graphics coprocessor 20 and to send "results" signals to main processor 12 to indicate a successful data transfer from system memory 14 or an error occurrence. (col. 3, line 19-25). Therefore, it is believed that a substantial

reconstruction or redesign is required to combine the main processor 12 with PCI interface block 109 due to the various control signals mentioned above. In addition, the PCI block interface 109 would require a substantial reconstruction or redesign because the PCI block interface 109 is configured to communicate with a register programming sequencer 108, a DMA arbiter 107 and EEPROM interface 110. (Munson '277, Figure 4). Moreover, if PCI block interface 109 is simply added to bus 22, as the Examiner suggests, then the resulting combination would be non-operative because two bus masters (graphics coprocessor 20 and PCI block interface 109) would be competing against each other during data transfer functions along bus 22. Therefore, the combination of Hancock '514 and Munson '277 is improper.

The Examiner also correctly states that Munson '277 fails to expressly teach a receiving method of video data in contiguous successive streams of luminance and chrominance difference data. In an attempt to overcome the deficiency of Munson '277, the Examiner relies on Coelho '137 to show an alleged technique for formatting YUV9 subsampled data, wherein

a frame buffer is divided into plural blocks for storing sequential packed video stream data (Y,U,V).

Coelho '137 discloses a system including a memory buffer 301 for storing YUV data in the planar format. A video processor 302 converts the planar YUV data into packed (interleaved) YUV data and a digital graphics display controller 304 receives the video processor 302 output in order to drive a monitor 305. Coelho '137 does not disclose or suggest a bus interface and a display memory controller having features as recited above in claim 1. Therefore, the Applicant respectfully submits that claim 1 is patentably distinguishable over Coelho '137.

As stated above, the combination of Hancock '514 and Munson '277 is improper. Furthermore, there is no suggestion or incentive to combine Hancock '514 and Munson '277 and Coelho '137 for the following reasons. First, it is believed that a substantial reconstruction or redesign is required for the combination of main processor 12, write mode register 42 and video memory access controller 28 in Hancock '514, in order to set a pixel state mask for a corresponding pixel data in a packed YUV format. Second, a substantial modification or

redesign of the data processing system 10 of Hancock '514 is required if the graphics coprocessor 20 of Hancock '514 is replaced by Coelho's video processor 302 which is programmed to convert planar data to packed YUV data. As stated above, the graphics coprocessor 20 of Hancock '514 is configured for receiving "control commands" from and sending "results" signals to the main processor 12. Therefore, the combination of Hancock '514, Munson '277 and Coelho '137 is improper.

The Applicant further submits that isolated disclosures in the prior art cannot be combined where there is no suggestion or incentive to do so. The CAFC has repeatedly noted that:

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under Section 103, teachings of references can be combined only if there is some suggestion or incentive to do so. The prior art of record fails to provide any such suggestion or incentive. (Emphasis original). ACS Hospital Systems, Inc. v. Montefiore Hospital, 231 U.S.P.Q. 929, 933 (C.A.F.C. 1984).

In the instant case there is no suggestion or incentive to combine Hancock '514, Munson '277, and Coelho '137 as the Examiner has suggested. Once cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to duplicate the claimed invention.

Assuming for the sake of argument that there is a suggestion to combine, the combination of Hancock '514, Munson '277, and Coelho '137 does not equal the claimed invention. The combination of Hancock '514, Munson '277, and Coelho '137 provides, at best, a system that includes a video memory access controller for providing pixel data values and pixel state values to a video memory, and that further includes <u>two</u> bus masters for controlling a single bus 22, and that further includes a video processor for converting planar YUV data into "packed" (interleaved) YUV format. Thus, the combination of Hancock '514, Munson '277 and Coelho '137 does not yield the Applicant's claimed invention, since the Applicant recites in claim 1, a display controller including a bus interface and a display memory controller with the following features and capabilities: ***(1) receiving video data in a component YUV format in contiguous successive streams of luminance and***

chrominance difference data and corresponding video data addresses within a predetermined address range; and (2) storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory; and (3) storing the first contiguous block of luminance data in at least one byte lane within the display memory and storing the at least a second contiguous block of chrominance difference data in at least another byte lane within the display memory, and no such display controller is described in any of the cited art.

The Examiner also correctly states that the references of Hancock '514, Munson '277, and Coelho '137 fail to teach a bit block transfer engine for performing a replicating function. In an attempt to overcome the above deficiency, the Examiner relies on Selwan '025 to show an apparatus and method "for performing run length tagging by the use of BITBLT circuit (1106), BITBLT tag generation circuit block (1202), FIFO controller (1220) sending a signal on bus

(1228) to alert display memory controller (1210) to stop loading data at FIFO full condition".

Fig. 11 in Selwan '025 discloses a VGA accelerator display controller that includes a CPU bus interface and write buffer 1102, a graphics controller 1104, a BITBLT and FIFO block 1106, a CRT controller block 1108, and a display memory sequencer block 1110. The display memory sequencer block 1110 further comprises a display memory controller 1122. Data is sent from BITBLT and FIFO block 1106 to display memory controller 1122. The pixel FIFO 1124 (in display sequencer block 1110) receives data bursts from a display memory through display memory controller 1122 which are to be output to the CRT. (col. 17, lines 58-66). Selwan '025 does not disclose or suggest, as recited in claim 1, a display controller including a display memory controller with the features described above.

Furthermore, the combination of Hancock '514, Munson '277, Coelho '137, and Selwan '025 does not yield the Applicant's claimed invention, since the Applicant recites in claim 1, a display controller including a bus interface and a display memory controller with the features described above.

Hancock '514 does not disclose, as substantially recited in claim 12, the steps of: (a) receiving, in a display controller, video data in a component YUV format in contiguous successive streams of luminance and chrominance difference data and corresponding video data addresses within a predetermined address range, (b) storing the video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory,..... and (c) storing, by use of a display memory controller, the first contiguous block of luminance data in at least one byte lane within the display memory and the at least a second contiguous block of chrominance difference data in at least another byte lane within the display memory.

As also discussed above, the combination of Hancock '514, Munson '277, and Coelho '137 is improper. Additionally, for the same reasons stated above, Hancock '514, Munson '277, Coelho '137, and Selwan '025, either alone or in combination, do not yield the Applicant's claimed invention which includes the steps recited in the previous paragraph. For example, the

combination of Hancock '514, Munson '277, and Coelho '137 provides, at best, a method that includes the steps of storing pixel data and pixel state values in a video memory by use of a video memory access controller, using a video display controller to continuously access the pixel data in the video memory one pixel at a time, and converting planar YUV data into a "packed" (interleaved) YUV format.

Since dependent claims 5-11 and 16-22 depend from various ones of claims 1 and 12 and include all limitations thereof, the dependent claims also patentably distinguish over Hancock '514, in view of Munson '277, further in view of Coelho '137, and further in view of Selwan '025, for at least the same reasons that independent claims 1 and 12 distinguish over the same references. The patentability of claims 5-11 and 16-22, however, does not depend on the patentability of their respective base claims, inasmuch as each dependent claim recites an additional feature which, in combination with the features recited in the base claims, are not disclosed by the cited references. For example, dependent claim 7 recites the at least one byte lane as comprising a plurality of adjacent byte lanes, each pair of the plurality of pairs of byte lanes

for storing pairs of luminance data for one line of one frame of video data. The above feature of dependent claim 7 is not recited in the above cited references.

The Applicant respectfully submits that claims 1, 5-12, and 16-22 are now patentably distinguishable from the cited reference. In view of the above claim amendments and remarks, the applicant respectfully requests allowance of claims 1, 5-12, and 16-22.

Respectfully submitted,

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DATE: June 25, 1999 BY: _____

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